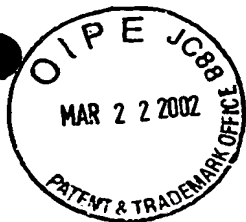


Case No. 00GR35154360



DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE
WASHINGTON, DC 20231

In re Application of: **COFLER ET AL.**

Serial No.: **10/082,816**

Filed: **FEBRUARY 25, 2002**

For: **METHOD OF HANDLING BRANCHING INSTRUCTIONS WITHIN
A PROCESSOR, IN PARTICULAR A PROCESSOR FOR DIGITAL
SIGNAL PROCESSING, AND CORRESPONDING PROCESSOR**

Sir:

Transmitted herewith is an INFORMATION DISCLOSURE STATEMENT in the above-identified application.

1. ☒ This IDS is submitted under 37 C.F.R. § 1.97. No fee is required.
2. ☐ This IDS is submitted under 37 C.F.R. § 1.97(c). Enclosed is a check in the amount of \$ 180.00.
3. ☐ This IDS is submitted under 37 C.F.R. § 1.97(c) and (e). No fee is required.
4. ☐ This IDS is submitted under 37 C.F.R. § 1.97(d) and (e). Enclosed is a check in the amount of \$ 130.00 to cover the petition fee.
5. ☒ **The Commissioner is hereby authorized to charge or credit any discrepancies in fee amounts to Deposit Account No. 01-0484.**

Date: March 13, 2002



CHRISTOPHER F. REGAN
Reg. No. 34,906



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
COFLER ET AL.)
Serial No. 10/082,816)
Filing Date: FEBRUARY 25, 2002)
For: METHOD OF HANDLING BRANCHING)
INSTRUCTIONS WITHIN A PROCESSOR,)
IN PARTICULAR A PROCESSOR FOR)
DIGITAL SIGNAL PROCESSING, AND)
CORRESPONDING PROCESSOR)

CITATION UNDER 37 CFR \$1.97(c)

Director, U.S. Patent and Trademark Office
Washington, DC 20231

Sir:

Attached is a form PTO-1449 listing several references for consideration in the examination of the above-identified application. A copy of each reference is also enclosed. It is requested that these references be considered by the Examiner and officially made of record in accordance with the provisions of 37 CFR \$1.97 and Section 609 of the MPEP.

Respectfully submitted,

CHRISTOPHER F. REGAN

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In Re Patent Application of:

COFLER ET AL.

Serial No. 10/082,816

Filing Date: 02/25/02



CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, DC 20231**, on this 13th day of March, 2002.

Dawn Finley

**INFORMATION DISCLOSURE
STATEMENT**Atty Docket:
Serial No.:
Applicant:
Filing Date:
Group:00GR35154360
10/082,816
COFLER ET AL.
02/25/2002**U.S. PATENT DOCUMENTS**

Examiner Initials		Document Number	Date	Name	Class	Sub Class	Filing Date
	AA	4,827,402	05/02/89	Wada	364	200	04/22/86
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub Class	Translation
	AK	0 133 477	02/27/85	EP	G06F	9/38	
	AL	0 689 131	12/27/95	EP	G06F	9/38	
	AM	0 840 209	05/06/98	EP	G06F	9/38	
	AN	1 050 805	11/08/00	EP	G06F	9/38	
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	Moore C.R. "The Power PC™ 601 Microprocessor"; proceedings of the spring computer society international conference, San Francisco, CA published on February 22, 1993, Publication No. XP000379036; pages 109-116
	AR	Toyohiko Yoshida et al., "A Strategy for Avoiding pipeline Interlock Delays in a Microprocessor", published by LSI Research and Development Laboratory on September 17, 1990; Publication No: XP 000201400; pages 14-19; ISBN: 0-8186-2079-X.
	AS	

EXAMINER:**DATE CONSIDERED:**

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.